

WHAT IS CLAIMED IS:

- 5 *Sub A1*
1. A method of manufacturing a semiconductor device comprising steps of:
 - (a) forming an etching object on a semiconductor substrate;
 - (b) forming a first resist film on said etching object;
 - (c) patterning said first resist film to obtain a first resist pattern;
 - (d) performing ion implantation into said first resist pattern, the thickness of said first resist pattern contracting by said ion implantation in said step (d); and
 - (e) executing predetermined etching on said etching object using said first resist pattern as a mask to obtain a work pattern, after execution of said steps (c) and (d), wherein
 - 10 the thickness of said first resist pattern after execution of said step (d) is set to a level satisfying such a condition that difference in critical dimension shift in said work pattern with respect to said first resist pattern caused between a dense pattern portion and
 - 15 a rough pattern portion in said work pattern is not more than a predetermined reference value and causes no hindrance to said predetermined etching.
 2. The method of manufacturing a semiconductor device according to claim 1, wherein
 - 20 said etching object includes an actual etching object and an ion prevention film, said step (a) includes steps of:
 - (a-1) forming said actual etching object on said semiconductor substrate, and
 - (a-2) forming said ion prevention film on said actual etching object,
 - 25 said ion implantation in said step (d) includes ion implantation from above said first resist pattern, and

said ion prevention film prevents ions implanted in said step (d) from being implanted into said actual etching object.

3. The method of manufacturing a semiconductor device according to claim 2,
5 wherein

said ion prevention film includes a silicon nitride film or a silicon oxynitride film, and

said step (a-2) includes a step of forming said ion prevention film by plasma CVD.

4. The method of manufacturing a semiconductor device according to claim 2,
wherein

said ion prevention film includes an organic antireflection coating.

5. The method of manufacturing a semiconductor device according to claim 4,
wherein

said step (a) further includes a step of:

(a-3) performing ion implantation into said organic antireflection coating forming said ion prevention film.

6. The method of manufacturing a semiconductor device according to claim 1,
wherein

said etching object includes first and second work areas,

said first resist pattern includes a pattern for an etching mask for said first work

25 area,

said method further includes steps of:

(f) forming a second resist film at least on said second work area after execution of said step (d), and

(g) patterning said second resist film to obtain a second resist pattern for an etching mask for said second work area, and

said step (e) includes a step of executing said predetermined etching using said second resist pattern as a mask in addition to said first resist pattern.

7. The method of manufacturing a semiconductor device according to claim 6, wherein

said step (f) includes a step of forming said second resist film on the overall surface of said etching object including said first pattern, and

said first resist pattern is not substantially removed in execution of said step (g) due to composition change resulting from said ion implantation in said step (d).

8. The method of manufacturing a semiconductor device according to claim 1, wherein

said ion implantation in said step (d) includes ion implantation performed obliquely from above with respect to a vertical line a surface formed with said first resist pattern.

9. The method of manufacturing a semiconductor device according to claim 1, wherein

said etching object has asperities on its surface, and

said method further comprises a step of:

(h) performing ion implantation into said etching object before executing said step (b).

10. The method of manufacturing a semiconductor device according to claim 5 9, wherein

said step (b) includes a step of performing exposure on said first resist film through a reticle of a predetermined pattern and thereafter executing development thereby obtaining said first resist pattern.

10 11. The method of manufacturing a semiconductor device according to claim 9, wherein

said etching object has a mark for mask alignment on its surface.

15 12. The method of manufacturing a semiconductor device according to claim 11, wherein

said step (h) includes steps of:

(h-1) forming a third resist film on said etching object,

(h-2) patterning said third resist film to obtain a third resist pattern, said third resist pattern having an opening on a mark forming region including said mark, and

20 (h-3) performing ion implantation into said mark forming region of said etching object using said third resist pattern as a mask.

13. The method of manufacturing a semiconductor device according to claim 1, wherein

25 said ion implantation in said step (d) includes a plurality of partial ion

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implantation operations different in implantation energy from each other.

14. A method of manufacturing a semiconductor device comprising steps of:

(a) forming an etching object on a semiconductor substrate;

(b) forming a first resist film on said etching object;

(c) patterning said first resist film to obtain a first resist pattern;

(d) performing chemical reaction acceleration for accelerating decomposition on said first resist pattern;

(e) performing curing including one of ion implantation, electron beam irradiation and ultraviolet irradiation on said first resist pattern, the thickness of said first resist pattern contracting by said curing in said step (e); and

(f) executing predetermined etching on said etching object using said first resist pattern as a mask to obtain a work pattern after execution of said steps (c) to (e).

15. The method of manufacturing a semiconductor device according to claim 14, wherein

said etching object includes first and second work areas,

said first resist pattern includes a pattern for an etching mask for said first work area,

said method further includes steps of:

(g) forming a second resist film at least on said second work area after execution of said step (e), and

(h) patterning said second resist film to obtain a second resist pattern for an etching mask for said second work area, and

said step (f) includes a step of executing said predetermined etching using said

second resist pattern as a mask in addition to said first resist pattern.

16. The method of manufacturing a semiconductor device according to claim 15, further comprising steps of:

- 5 (i) performing chemical reaction acceleration for accelerating decomposition at least on said second resist pattern before said step (f) and after said step (h), and
- (j) performing said curing at least on said second resist pattern before said step (f) and after said step (h).

10 17. The method of manufacturing a semiconductor device according to claim 14, wherein

said chemical reaction acceleration includes at least either exposure or heat treatment on said etching object.

15 18. A method of manufacturing a semiconductor device comprising steps of:

(a) forming an etching object having first and second work areas on a semiconductor substrate;

(b) forming a first resist film on said etching object;

20 (c) patterning said first resist film to obtain a first resist pattern on said first work area;

(d) performing curing including one of ion implantation, electron beam irradiation and ultraviolet irradiation on said first resist pattern, the thickness of said first resist pattern contracting by said curing in said step (d);

25 (e) forming a second resist film at least on said second work area after execution of said step (d);

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Figure 1. The effect of the number of trials on the number of correct responses. The number of correct responses was plotted against the number of trials for each condition. The number of correct responses increased with the number of trials for all conditions. The number of correct responses was highest for the condition with the highest number of trials (10 trials) and lowest for the condition with the lowest number of trials (2 trials).